Abstract of Disclosure

The inventive ferroelectric memory device includes: a semiconductor substrate providing elements of a transistor; a first inter-layer insulating layer formed on the semiconductor substrate; a storage node contact connected to elements of the transistor by passing through the first inter-layer insulating layer; a barrier layer contacting simultaneously to the storage node contact and the first inter-layer insulating layer; a lower electrode having a space for isolating the first inter-layer insulating layer and being formed on the barrier layer; a glue layer being formed on the first inter-layer insulating layer and encompassing lateral sides of the lower electrode as filling the space; a second inter-layer insulating layer exposing a surface of the lower electrode and encompassing the glue layer; a ferroelectric layer formed on the glue layer including the second inter-layer insulating layer; and an upper electrode formed on the ferroelectric layer.